DETAILED ACTION

Response to Amendment

1. This office action has been issued in response to the amendment filed 08/25/10. Claims 1-23 are pending in this application. Applicant's arguments have been carefully considered, but are not persuasive in view of the prior art as applied to a broadest reasonable interpretation of the claims and/or moot in view of new grounds of rejection. The examiner appreciates Applicant's effort to distinguish over the cited prior art by amending the claims to more clearly describe the invention, however, upon further consideration and/or search, the claims remain unpatentable over the cited prior art. All claims pending in the instant application remain rejected and clarification and/or elaboration regarding why the claims are not in condition for allowance will hereafter be provided in order to efficiently further prosecution. Accordingly, this action is made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-23 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Robertson (US Patent # 6,892,253) in view of Myers (US Patent # 2002/0146023) further in view of Bender et al. (US Patent # 5,664,223).

With respect to **independent claims 1, 7, 12, 18** Robertson discloses a device (*Robertson - fig. 4*) for writing data elements from a coprocessor [*understood as one or more functional/logic elements*

capable of performing processing] into a FIFO memory, in a multiprocessing environment [*understood as an environment comprising more than one processing elements*] comprising at least one coprocessor, a FIFO memory and a controller [*understood as one or more functional/logic components capable of controlling other system components*], said device comprising:

a first counter implemented within the coprocessor, [*master count 251 (Robertson – abstract), the claimed coprocessor is understood to be any arrangement of functional elements/logic described in the cited art which are able to function in a processing capacity*] the first counter for counting the available room in said FIFO memory, wherein the FIFO memory is located remotely from the coprocessor [*FIFO buffer 410 is separated from the functional components understood to make up the claimed coprocessor (Robertson Fig. 4)*], [*FIFOs are separate from functional components (Myers Fig. 9)*];

a second counter implemented within the coprocessor [*remote count 252 (Robertson – abstract), understood to be grouped with functional elements capable of performing processing*] the second counter for counting the number of data elements written into said FIFO memory, wherein the data elements are at least part of a communication between the coprocessor and the controller in the multiprocessing environment [*data elements pass through control and processing components on their way to a FIFO at least in Fig. 2 of Robertson*];

control means implemented within the coprocessor [*Robertson Fig. 1, 2 ,4*] and coupled to the first and second counters, wherein the control means is configured for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory [*Robertson – abstract, Fig. 1-2 & 4*]; and

output means implemented within the coprocessor, the output means for outputting data elements to said FIFO memory [*since remote count indicates the number of entries stored in the FIFO buffer (Robertson – abstract, Col 7 lines 48-50), means for outputting/storing data elements into the FIFO are inherent in the disclosure of Robertson's invention; see also fig. 4 of Robertson where the pipeline stages output data to the FIFO buffer 410*], wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller [*Robertson suggests the claimed element arrangement or orientation in Fig. 1-2, but appears not to explicitly disclose the claimed arrangement*];

wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N [*Upon allocation of N (some variable number) data items into the FIFO buffer, an output signal may be asserted when N is equal to some threshold value (Robertson – Col 5 lines 7-30)*] by incrementing of the count of said second counter after a data element has been written into said FIFO memory [*remote count 252 is incremented upon allocation of data to the FIFO (Robertson - abstract)*];

wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*]; and

wherein said output means is adapted to forward said first message and/or said first call to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*], wherein the controller is located remotely from the coprocessor [*control components and processing components are understood to be remote from one another (Robertson Fig. 2,4)*].

Robertson does not **explicitly** disclose the claimed control means, output means, controller, FIFO and counter arrangement or interconnection although the claimed functionality of these elements is understood to be present in Robertson, just not in the particular order that applicant has claimed so that the claims do not extent beyond the scope of what one of ordinary skill would understand to be an obvious modification to Robertson.

In the same field of endeavor, Myers teaches a transport stream multiplexer utilizing smart FIFO meters wherein a broadest reasonable interpretation of applicant claimed functional element arrangement is disclosed (*Myers Fig. 1, 3, 9, 11*).

Therefore Robertson in view of Myers disclose wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller [*Myers Fig. 3, 9, 11*].

Robertson in view of Myers does not **explicitly** disclose the environment in which the invention is implemented - as in the preamble of the instant claim(s) – namely a processor/coprocessor environment.

Nevertheless, in the same field of endeavor Bender teaches the implementation of a FIFO similar to the one disclosed in Robertson's invention, but in a processor/coprocessor environment (*Bender – Col 2 lines 60-67, Col 4 lines 40-59*) including a controller (*Bender - Col 5 line 19*).

Therefore Robertson in view of Myers further in view of Bender discloses all limitations of the instant claim(s).

It would have been obvious to one having ordinary skill in the art at the time of the invention to include means for performing a signaling operation when the count of a counter has been incremented by N in the invention of Robertson because it would be advantageous to signal that a fullness/emptiness threshold has been exceeded before the FIFO is actually full/empty since hardware delays and latency properties may not allow a less forgiving implementation to prevent the FIFO from overflowing / underflowing (*Robertson – Col 5 lines 7-20, abstract*). Moreover, it would be advantageous to include means for performing a signaling operation when the count of a counter has been incremented by N to assist with timing of transfer operations into/out from a FIFO memory for the purpose of achieving load balancing in the case of a plurality of FIFO memories (*this understanding is supported/evidenced by Myers – US Patent # 6,877,049 – abstract, and/or Myers – US Patent # 2002/0146023 – paragraph 0012-0013*). Lastly, it would have been obvious to one of ordinary skill in the art at the time of the invention to arrange the functional elements such that they would be interconnected as claimed and as shown in Fig. 3, 9, 11 of Myers because not only would the interconnection facilitate the proper operation of the invention, but also because the number of ways that 5 functional components may be interconnected is finite, and it would have been within the purview of a skilled artisan to select one of several know and finite interconnections for a plurality of functional elements.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a FIFO (as part of a decoupling mechanism) in a processor/coprocessor environment in the invention of Robertson as taught by Bender because it would be advantageous to decouple a main processor from certain operations which are cumbersome and which may be (offloaded on/assigned to) a supporting co-processor (*Bender – Col 1 lines 25-37*) thereby effecting more efficient and expedient system operation.

With respect to independent claims 12, 18 Robertson's in view of Bender invention is capable of performing the steps of the claimed method and includes all elements of the claimed device since reading and writing are symmetric operations as is well known by the applicant (paragraph [0006] of applicant's specification). Is well known to one of ordinary skill in the art that reading and writing are symmetric I/O operations such that an exemplary disclosure wherein operations are performed with respect to writing data, would render a symmetric disclosure of operations being performed with respect to reading data an obvious variant.

With respect to **dependent claim 2, 13** as applied to claim 1, 12 above, Robertson in view of Bender discloses said first message indicates that sufficient data elements have been written into said FIFO memory [*Robertson – Col 7 lines 7-30*], [*main processor on the outgoing side will move the packet*

into its outgoing FIFO and will inform the coprocessor by putting a message into its memory (Bender - Col 10 lines 16-18)].

With respect to **dependent claims 3, 8, 14, 19** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses incrementing a write pointer, when data elements were output to said FIFO memory [*When data is put into the FIFO, the tail pointer is incremented and when data is taken out of the FIFO the head pointer is incremented (Bender - Col 10 lines 39-42)*].

With respect to **dependent claims 4, 9, 15, 20** as applied to claims 3, 8, 14, 19 above, Robertson in view of Bender discloses performing a wrap-around test after said write pointer was incremented [*check to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 4-6)*].

With respect to **dependent claims 5, 10, 16, 21** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses resetting said second counter after issuing said first message [*Robertson – Col 7 lines 47-62*], [*a reset device, operatively coupled to said output of the counting mechanism, for resetting the adaptor; and a reset transmitting device, operatively coupled between the reset device and the main processor for transmitting the reset condition of the adaptor to the main processor (Bender - Col 3 lines 35-40)*].

With respect to **dependent claims 6, 11, 17, 22** as applied to claims 1, 7, 13, 18 above, Robertson in view of Bender discloses issuing said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero [*Robertson – Col 5 lines 7-30*], [*it first polls the head pointer in its local memory and compares it with its cached value of the tail pointer to determine if there is space in the outgoing FIFO... checks to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 2-6); If it is full, local polling occurs at the coprocessor. While there is polling occurring, the main processor can send a new "receive head" through the adaptor to thereby update the "receive head" in the coprocessor 22. (Bender - Col 13 lines 10-14). Note that issuing the call before the count of first counter becomes zero is understood to be functionally equivalent to setting a predetermined threshold value which indicates an almost full state for the FIFO queue and issuing the call based on the counter or pointer reaching that value*].

With respect to **dependent claim 23** as applied to claim 1 above Robertson in view of Bender discloses a Multiprocessing computer system, comprising: a FIFO memory; at least one coprocessor; a controller, a device for writing according to claim 1 [*See rejection of claim 1 above*].

Response to Arguments

5. Applicant's arguments filed 08/25/10 have been fully considered but are not persuasive in view of the prior art and/or moot in view of new ground(s) of rejection necessitated by amendment to the claims. All claims pending in the instant application remain rejected. Please note that any rejections/objection not maintained from the previous Office Action have been rectified either by applicant's amendment and/or persuasive argument(s).

6. New grounds of rejection necessitated by amendments to the claims render the remarks moot and/or unpersuasive. The examiner would like to note that because the claims do not define what the coprocessor and controller are, the new limitations regarding what components are implemented within the coprocessor or controller are substantially non-limiting. In other words, in accordance with a broadest reasonable interpretation of the claimed controller and coprocessor, these limitations are understood to correspond to any arrangement of functional/logic components in the prior art which are capable of performing processing or control functions.

Conclusion

When responding to the office action, **any new claims and/or limitations should be accompanied by a reference as to where the new claims and/or limitations are supported in the original disclosure**.

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash whose telephone number is 571-270-1179. The examiner can normally be reached on Mon-Fri 9am-6pm. The examiner may be reached via email for unofficial correspondence at marwan.ayash@uspto.gov.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/02/10 Marwan Ayash - Examiner - Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185